WHAT IS CLAIMED IS:

1. A method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, at least one instruction address of or data address being part of the pseudo instruction, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction;

prefetching the instruction or data from the memory in accordance with the at least one instruction address or the data address; and

storing the prefetched instruction or data in a buffer.

2. The method of claim 1, further comprising a step of providing a pseudo instruction detection unit connected in parallel with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the memory to the pseudo instruction detection unit in parallel with the buffer.

3. The method of claim 1, wherein the buffer includes first and second buffers connected in parallel with the memory, and the method further comprising a step of storing the instruction and data read from the memory in the first buffer and storing the prefetched instruction or data in the second buffer.

4. The method of claim 3, wherein the step of

prefetching the instruction and data from the memory includes the steps of:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer when the pseudo instruction is detected; and

prefetching the instruction or data from the memory in accordance with the at least one instruction address or data address after the transfer of the at least one instruction to the first buffer has been identified.

5. The method of claim 3, further comprising the step of identifying that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction or data is not stored in the second buffer.

6. The method of claim 1, wherein the step of prefetching the instruction and data from the memory includes the steps of:

identifying that at least one instruction following the pseudo instruction has been transferred to the buffer when the pseudo instruction is detected; and

prefetching the instruction or data from the memory in accordance with at least one instruction address or data address after the transfer of at least one instruction to the buffer has been identified.

7. The method of claim 6, further comprising the step of identifying that the corresponding instruction or data is stored in the buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected, wherein the prefetch step is executed

when the corresponding instruction or data is not stored in the buffer.

8. A microcontroller, comprising:

a buffer, connected to a memory, for storing instructions and data of a program prefetched from the memory, wherein the program includes a pseudo instruction, at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, and at least one instruction address or data address being part of the pseudo instruction;

an instruction execution unit, connected to the buffer, for receiving the instruction and data from the buffer and executing a predetermined processing operation using the instruction and data;

a pseudo instruction detection unit, connected to the memory, for detecting the pseudo instruction included in the program prefetched from the memory; and

an address control unit, connected to the external memory and the pseudo instruction detection unit, for prefetching the instruction or data in accordance with at least one instruction address or data address when the pseudo instruction is detected.

9. The microcontroller of claim 8, wherein the buffer includes first and second buffers connected in parallel with the memory, wherein the first buffer stores the instruction and data prefetched from the memory, and the second buffer stores the instruction or data prefetched by the address control unit.

10. The microcontroller of claim 9, wherein the address control unit identifies that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected and permits storage of the instruction or data in the second buffer when the corresponding instruction or data is not stored in the second buffer.

11. The microcontroller of claim 10, wherein the pseudo instruction detection unit is connected in parallel with the first buffer for the memory.

12. The microcontroller of claim 8, wherein the address control unit identifies that the corresponding instruction or data is stored in the buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected and permits storage of the instruction or data in the buffer when the corresponding instruction or data is not stored in the buffer.

13. The microcontroller of claim 12, wherein the pseudo instruction detection unit is connected in parallel with the buffer for the memory.

14. A device for detecting a pseudo instruction preset before a specific instruction, wherein the pseudo instruction includes an opcode and an operand, the device comprising:

a detection circuit, connected to a data line, for receiving the pseudo instruction transferred on the data line and detecting the opcode included in the pseudo instruction; and

a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode and

determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for validating the opcode detection operation during an operand transfer period.

15. A recording medium having a program stored thereon, wherein the program includes a pseudo instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, and wherein the at least one instruction address or data address is part of the pseudo instruction.

16. A microcontroller connected to a memory which stores instructions and data, the microcontroller comprising:

an instruction execution unit for reading instructions and data from the memory and processing the read instructions; and

a prefetch circuit unit that receives instructions and data read from the memory in response to a fetch signal, and detects pseudo instructions included in the instructions and data, wherein a pseudo instruction precedes a branch instruction and indicates the existence of the branch instruction;

wherein the prefetch circuit unit includes,

a prefetch buffer connected between the instruction execution unit and the memory for temporarily storing instructions and data being transferred from the memory to the instruction execution unit,

a bus interconnecting the prefetch buffer and the memory,

a pseudo instruction detection unit connected to the

bus for detecting pseudo instructions among the instructions and data being transferred from the memory to the prefetch buffer,

a holding circuit, connected to the bus and to the pseudo instruction detection unit, for storing operands of the pseudo instruction,

a pseudo instruction buffer for temporarily storing instructions and data fetched from a location in the memory which is pointed to by the branch instruction following the pseudo instruction,

an address control unit for generating the fetch signal and for generating a memory address which points to the address of a next word to be read from the memory, and wherein when the pseudo instruction detection unit detects a pseudo instruction, the instructions and data pointed to by the pseudo instruction are fetched from the memory by the address control unit and stored in the pseudo instruction buffer so that when the branch instruction following the pseudo instruction is processed by the instruction execution unit, if the branch is taken, the instructions and data pointed to by the branch instruction have been prefetched and stored in the pseudo instruction buffer.

17. The microcontroller of claim 16, wherein the pseudo instruction detection unit further comprises:

a pseudo instruction detection circuit that receives at least a part of each of the instructions and data being transferred from the memory to the prefetch buffer, detects an opcode of a pseudo instruction therefrom, and generates a detection signal; and

a shift register connected to the pseudo instruction detection circuit and receiving the detection signal, and generating a hold circuit enable signal, wherein when the hold circuit enable signal is active, the holding circuit stores

the pseudo instruction operands being transferred on the bus.

18. The microcontroller of claim 17, wherein the holding circuit includes:

an additional information holding circuit that stores a first operand of the pseudo instruction;

an upper address holding circuit that stores a second operand of the pseudo instruction; and

a lower address holding circuit that stores a third operand of the pseudo instruction, wherein the second and third operands comprise a memory address.